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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,629	11/17/2003	Frederic Boutaud	7020	4322

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EXAMINER	
LAI, VINCENT	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,629	BOUTAUD, FREDERIC	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/2/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 3/2/2005 was considered by the examiner.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Element 180 of figure 15 is not referenced in the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: Figure 18 is not listed under the section "Brief Description of the Drawings."

Appropriate correction is required.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Digital Signal Processor Architecture with Optimized Memory Access For Code Discontinuity".

Claim Objections

5. Claims 1-5, and 9-14 are objected to because of the following informalities:

Claim 1 recites the limitation "the operations" in lines 7-8. There is insufficient antecedent basis for this limitation in the claim. It is suggested to be changed to and assumed to read "operations."

In claim 9, the sub-numbering of the comprising steps is mislabeled as there are two step (d)'s and (e)'s. The repeated steps are assumed to be (f) and (g);

In claim 9, line 12, "loop" should read "the loop" since it was mentioned previously;

Appropriate correction is required.

Claims 13-14 are objected to because of the term "during a loop instruction" in line 2 of claim 13. The claim does not make grammatical sense. It is suggested to be changed to and assumed to read "during the execution of a loop instruction";

Claims 13-14 are also objected to because claim of the term "next instruction." It is suggested another term be used to prevent confusion as what type of next instruction is to be fetched. The next instruction is assumed to be the target instruction after completion of the loop and another iteration of the loop;

Claim 14 is objected to because the phrase "the method saves" in lines 1-2 is not proper. It is suggested to be changed to "the method further comprising the step of saving";

Claim 14 is also objected to because of the phrase "the method fetches" in lines 3-4. Methods cannot fetch. It is suggested to be changed to "the method comprises the step of fetching"; and

Claim 14 is further objected to because it claims that an instruction is saved in "a stack register" (line 2) while in claim 13, it is claimed that an instruction is saved in register (line 7). It is suggested "in a stack register" be changed to "in a register."

Claim Rejections - 35 USC § 112

6. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 6, and 9 refer to "single cycle" in line 3 of all three claims. It is unclear as to what sort of cycle it is referring to. It could conceivable be interpreted as a clock or an instruction cycle. It is suggested to be changed to and assumed to read "single instruction cycle."

Claims 1, 6, and 9 also refer to "such that all instructions are executed in a single cycle" in lines 2-3 of all three claims. It is unclear as to what is executed in a single cycle. It can be interpreted as the entirety of a program is executed in a single cycle or each individual instruction be executed in a single cycle. It is suggested to be changed to and assumed to read "such that each individual instruction is executed in a single instruction cycle."

Claim 1 refers to "the fetched program instruction" in step (d) (line 14) and it is unclear as to which fetched program it is referring to. It is suggested to be changed to and assumed to read "the fetched program instruction from the unified memory."

Claim 1 also refers to "the fetched program instruction" twice in step (e) (lines 18-19) and it is unclear as to which fetched program it is referring to. It is suggested to be changed to and assumed to read "the fetched program instruction from the first access of the unified memory."

Claim 4 refers to "the fetched program instruction" in line 2 and it is unclear as to which fetched program it is referring to. It is suggested to be changed to and assumed to read "the fetched program instruction from the first access of the unified memory."

Claim 6 refers to "the fetched program instruction" in step (b) (line 5) and it is unclear as to which fetched program it is referring to. It is suggested to be changed to and assumed to read "a fetched program instruction" since it is referring to a different fetched program instruction than the one mentioned in step a.

Claim 6 refers to "the program instruction" in step (c) and (d) (line 8 and 11, respectively) and it is unclear as to which program instruction it is referring to. It is suggested to be changed to and assumed to read "the fetched program instruction."

Claims 2-5, 7-8, 9-11 are rejected because they depend on claim 1, 6, and 9, respectively.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Morley (U.S. Patent # 4,276,594), herein referred to as Morley.

As per claim 1, Morley discloses a method for accessing a unified memory in a micro-processing system having a microprocessor, a one level pipeline and a two-phase clock such that all instructions are executed in a single cycle, comprising:

(a) fetching (See figure 19, and column 18, lines 33-40: A fetch must be done) a program instruction from the unified memory (Public Memory 33, see figure 5);

(b) determining (See column 1, lines 32-36: A decision is made to what sort of instruction was fetched) if the fetched program instruction would require three unified memory accesses during a single instruction cycle for proper execution of the fetched program instruction (See column 58, lines 17-20: Parallel fetching is allowed, which is necessary when three unified memory accesses are to be completed as specified in the application. Three accesses can be done if one of two parallel fetches accesses the

memory with two reads and the other fetch accesses the memory with just one read), proper execution of the fetched program instruction being the microprocessor performing the operations requested by the fetched program instruction in a single instruction cycle (See figure 28: Reads are done in one cycle);

(c) accessing the unified memory a first time, during the instruction cycle associated with the fetched program instruction, with a dummy access (See column 58, lines 17-20: During phase phi, updates are done during a fetch, which is what happens when a dummy access is executed as stated in the specification of the application) when it is determined that the fetched program instruction requires three unified memory accesses (See column 58, lines 17-20: Parallel fetching is allowed, which is necessary when three unified memory accesses are to be completed as specified in the application. Three accesses can be done if one of two parallel fetches accesses the memory with two reads and the other fetch accesses the memory with just one read) for proper execution of the fetched program instruction;

(d) fetching a next program instruction from an instruction register (See column 46, table 14: Op code is read from an instruction register), during the instruction cycle associated with the fetched program instruction, when it is determined that the fetched program instruction requires three unified memory accesses (See column 58, lines 17-20: Parallel fetching is allowed, which is necessary when three unified memory accesses are to be completed as specified in the application. Three accesses can be done if one of two parallel fetches accesses the memory with two reads and the other fetch accesses the memory with just one read) for proper execution of the fetched

program instruction (See column 46, table 14: Op code is the machine language code that dictates how instructions are to be completed and thus will determine the operations of the instructions); and

(e) accessing the unified memory a second time (See figure 28: On a read, there is two reads done), during the instruction cycle associated with the fetched program instruction, with a data access when it is determined that the fetched program instruction requires three unified memory accesses for proper execution of the fetched program instruction (See column 58, lines 17-20: Allows for parallel fetching, which is needed when three unified memory accesses are made, as specified in the application. Three accesses can be done if one of two parallel fetches accesses the memory with two reads and the other fetch accesses the memory with just one read).

As per claim 2, Morley discloses wherein the data access is a read data access (See figure 28: Read is one data access operation).

As per claim 3, Morley discloses wherein the data access is a write data access (See figure 28: Write is one data access operation).

As per claim 4, Morley discloses wherein the fetched program instruction is a last instruction of a loop (See column 41, line 64-column 42, line 1: Morley discloses that the code does not change during a loop operation and thus the last instruction of a loop should have already been fetched during the operation of a loop).

As per claim 5, Morley discloses wherein the instruction register is an instruction stack (See column 36, lines 43-46: Call instructions are placed in a stack) thereby enabling program instruction fetches for nested loops (See column 18, lines 33-39: Fetching of a nest of code (which can be a nested loop) is allowed).

As per claim 6, Morley discloses a method for accessing a unified memory in a micro-processing system having a microprocessor, a one level pipeline, and a two-phase clock, such that all instructions are executed in a single cycle, comprising:

(a) fetching (See figure 19, and column 18, lines 33-40: A fetch must be done) a program instruction from the unified memory (Public Memory 33, see figure 5) during a first instruction cycle;

(b) determining if the fetched program instruction for a second instruction cycle is a conditional program code discontinuity (See column 1, lines 32-36: A decision is made to what sort of instruction was fetched);

(c) accessing the unified memory a first time during the second instruction cycle with a dummy access (See column 58, lines 17-20: During phase phi, updates are done during a fetch, which is what happens when a dummy access is executed) when it is determined that the program instruction accessed for a second instruction cycle is a conditional program code discontinuity; and

(d) accessing the unified memory a second time (See figure 28: On a read, there is two reads done) during the second instruction cycle to read a new instruction when it

is determined the program instruction accessed for a second instruction cycle is a conditional program code discontinuity, thereby delaying the instruction access from the unified memory for the second instruction cycle by a half cycle (See figure 19: There is a phase gap between reads).

As per claim 7, Morley discloses wherein the conditional program code discontinuity is a jump instruction (See column 39, lines 3-7: Jump is a special instruction).

As per claim 8, Morley discloses wherein the conditional program code discontinuity is a call instruction (See column 36, lines 43-46: Call instructions are handled differently from other instructions).

As per claim 9, Morley discloses a method for accessing a unified memory in a micro-processing system having a microprocessor, a one level pipeline, and a two-phase clock, such that all instructions are executed in a single cycle, comprising:

(a) fetching (See figure 19, and column 18, lines 33-40: A fetch must be done) a program instruction from the unified memory (Public Memory 33, see figure 5);

(b) determining (See column 1, lines 32-36: A decision is made to what sort of instruction was fetched) if the fetched program instruction is a loop initiation instruction;

(c) storing (See column 46, table 14: Op code is stored in an instruction register) a first instruction of the loop in an instruction register when the fetched program instruction is a loop initiation instruction;

(d) executing the loop (See column 41, line 67-column 42, line 1: Loops are executed with a special case for single instruction loops);

(e) determining if a fetched instruction during the execution of the loop is a last instruction of the loop (See column 1, lines 32-36: A decision is made to what sort of instruction was fetched);

(f) accessing the unified memory a first time, during the instruction cycle associated with the fetched last instruction of loop, with a dummy access (See column 58, lines 17-20: During phase phi, updates are done during a fetch, which is what happens when a dummy access is executed);

(g) fetching the first instruction of the loop from the instruction register (See figure 19, and column 18, lines 33-40: A fetch must be done), during the instruction cycle associated with the fetched last instruction of loop; and

(h) accessing the unified memory a second time, during the instruction cycle associated with the fetched last instruction of loop, with a data access (See figure 28: On a read, there is two reads done).

As per claim 10, Morley discloses wherein the data access is a read data access (See figure 28: Read is one data access operation).

As per claim 11, Morley discloses wherein the data access is a write data access (See figure 28: Write is one data access operation).

As per claim 12, Morley discloses wherein the instruction register is an instruction stack (See column 36, lines 43-46: Call instructions are placed in a stack), thereby enabling program instruction fetches for nested loops (See column 18, lines 33-39: Fetching of a nest of code (which can be a nested loop) is allowed).

As per claim 13, Morley discloses a method for accessing a unified memory in a micro-processing system during a loop instruction, comprising:

(a) accessing (See figure 19, and column 18, lines 33-40: A fetch must be done, which accesses the memory) a program instruction from the unified memory (Public Memory 33, see figure 5) during a first instruction cycle;

(b) determining a type of program instruction (See column 1, lines 32-36: A decision is made to what sort of instruction was fetched);

(c) pre-fetching a next instruction from the unified memory (See figure 28: On a read there is two reads done, the second read being possible to be a pre-fetch);

(d) saving the pre-fetched instruction in a register when it is determined that the type of program instruction is a first instruction of a loop (See column 46, table 14: Op code is stored in an instruction register);

(e) fetching a next instruction from the register (See column 46, table 14: Op code is read from an instruction register) when it is determined that the type of program instruction is a last instruction of a loop;

(f) accessing the unified memory with a dummy access (See column 58, lines 17-20: During phase phi, updates are done during a fetch, which is what happens when a dummy access is executed) during execution of the last instruction of the loop; and

(g) accessing the unified memory, a second time, with a data access during execution of the last instruction of the loop (See figure 28: On a read, there is two reads done).

As per claim 14, Morley discloses wherein the method saves the pre-fetched instruction in a stack register (See column 36, lines 43-46: Call instructions are placed in a stack) when it is determined (See column 1, lines 32-36: A decision is made to what sort of instruction was fetched) that the type of program instruction is first instruction of a loop to enable nested loops and interruptible loops, and the method fetches a next instruction from the stack register (See column 46, table 14: Op code is read from an instruction register) when it is determined that the type of program instruction is a last instruction of the loop.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the art with

respect to digital signal processor architecture with optimized memory access for code discontinuity:

U.S. Patent # 5,623,311 to Phillips et al shows a MPEG video decoder having a high bandwidth memory.

U.S. Patent # 5,809,550 to Shukla et al shows a method and apparatus for pushing a cacheable memory access operation onto a bus controller queue while determining if the cacheable memory access operation hits a cache.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

vl
February 8, 2006

2/13/06

HENRY W. H. TSAI
PRIMARY EXAMINER